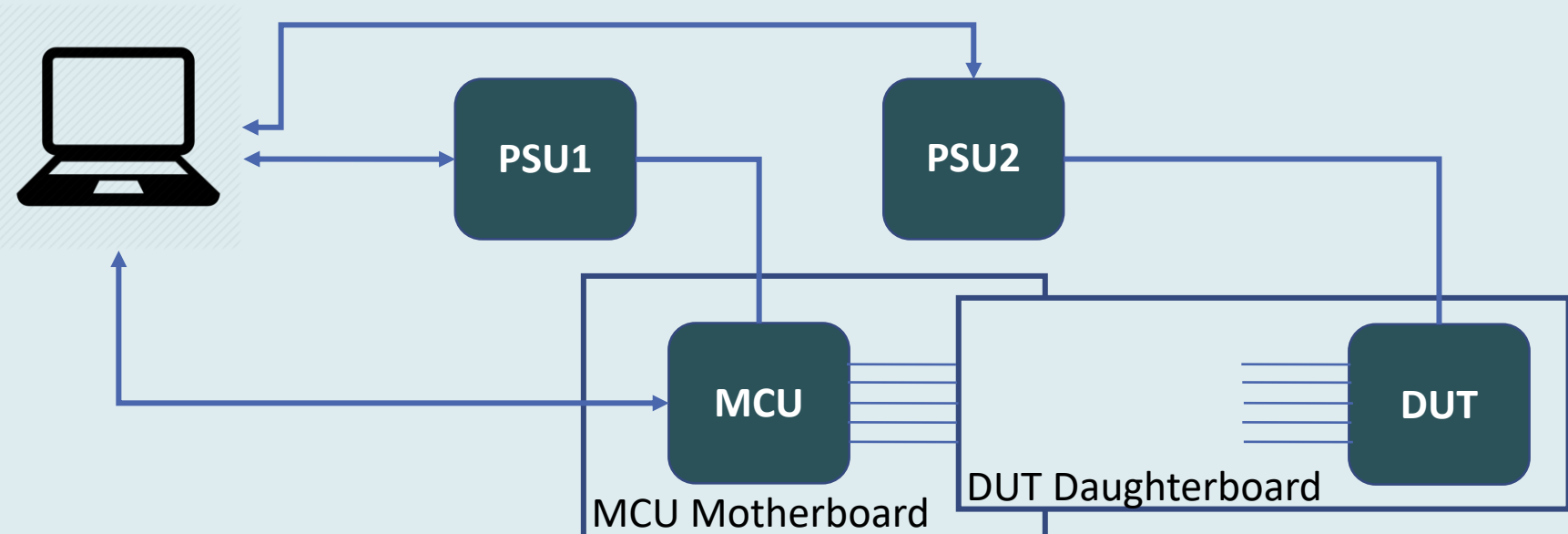# Radiation Testing of Memories

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Objectives:

- Identification and selection of appropriate test hardware
- Creation of C/C++ code for performing memory write and read operations
- Design of a test board suitable for both laser and heavy ion testing

Hardware Setup:

Devices Under Test (DUT):

Figure 1: A) 3D model of the test devices, B) schematic of the 24LC128 electrically erasable programmable read only memory (EEPROM), C) schematic of the 23LCV512 static random-access memory (SRAM) [1][2]

Background:

- Different types of memory ICs (integrated circuits) use different communication protocols, these protocols allow the memories to be accessed in order to perform read and write operations.
- Initial development was for both serial peripheral interface (SPI) and inter-integrated circuit (I^2C) communication protocols to enable SRAM, EEPROM and FLASH memories to be accessed.
- In order to test these memories against radiation, while the device is being irradiated an entire memory write is performed followed by an entire memory read. The difference between the written data and the read back data enables the location and number of bit upsets to be calculated.

Initial Testing and Code Development:

24LC128 EEPROM Development:

- The 24LC128 is a 128Kbit EEPROM device that uses I^2C as its communication protocol
- I^2C communication requires 2 wired connections: a serial clock line (SCK) which controls when the receiver samples the data, and a serial data line (SDA) which can send and receive the data.
- It can be seen in Figure 1B that the 24LC128 has 3 address pins (A0, A1, A2), these can be set either high or low and determine the address value of the chip. This allows up to 8 EEPROM devices to be run in parallel.
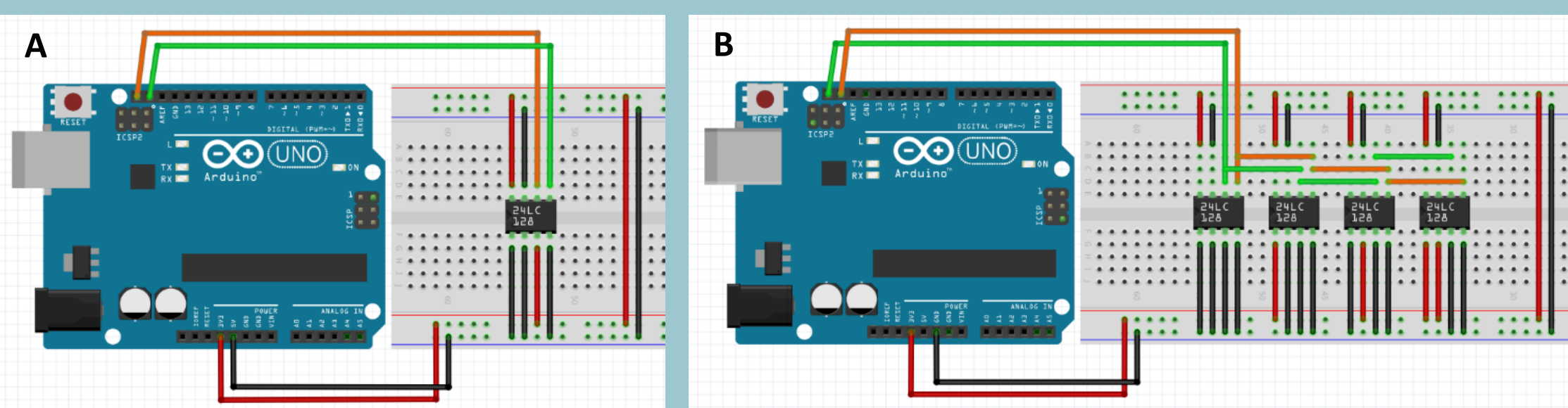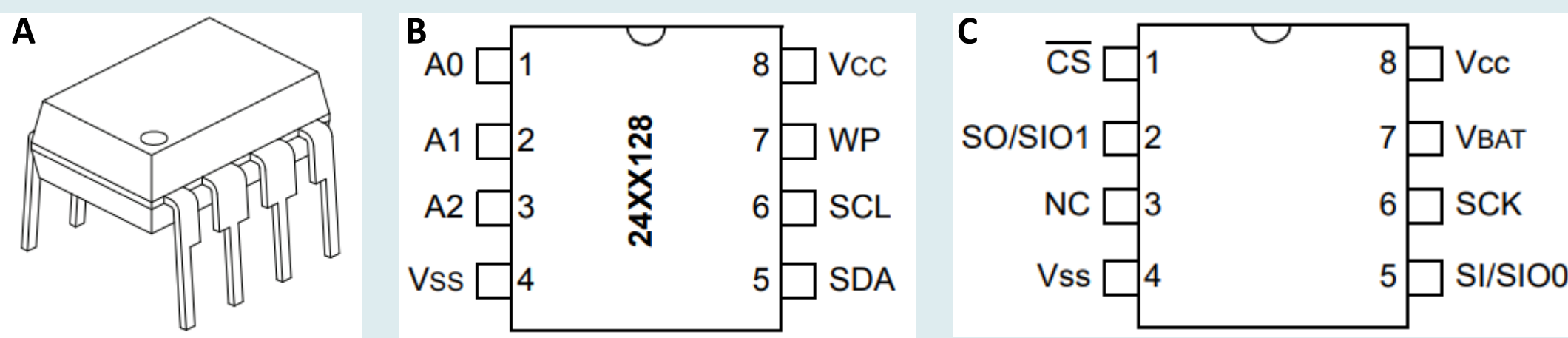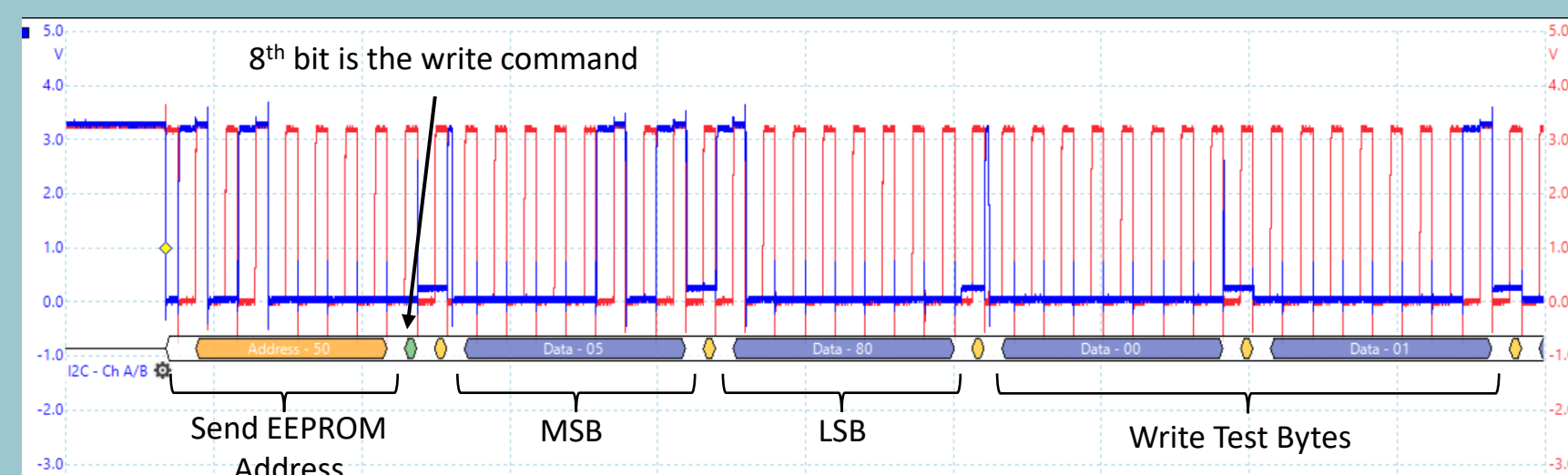
Figure 2: A) Single EEPROM circuit, B) Four EEPROMs connected in parallel

Figure 3: Waveforms of a write cycle to the EEPROM. ▨: SCK line ▨: SDA line
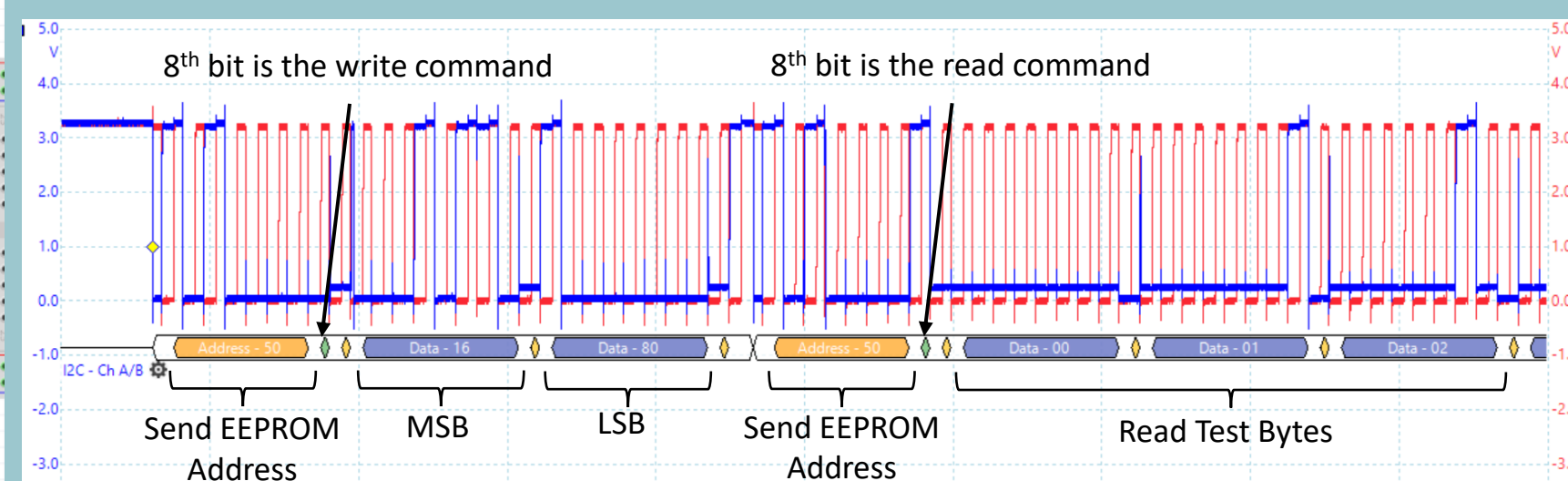
Figure 4: Waveform of a read cycle to the EEPROM.

23LCV512 SRAM Development:

- The 23LCV512 is a 512Kbit SRAM device that uses SPI as its communication protocol
- SPI communication requires 4 wired connections: a chip select line (CS) which enables multiple devices to be run simultaneously, a serial clock line (SCK), a master input slave output line (MISO) which receives data from the memory, and a master output slave input line (MOSI) which sends data to the memory.
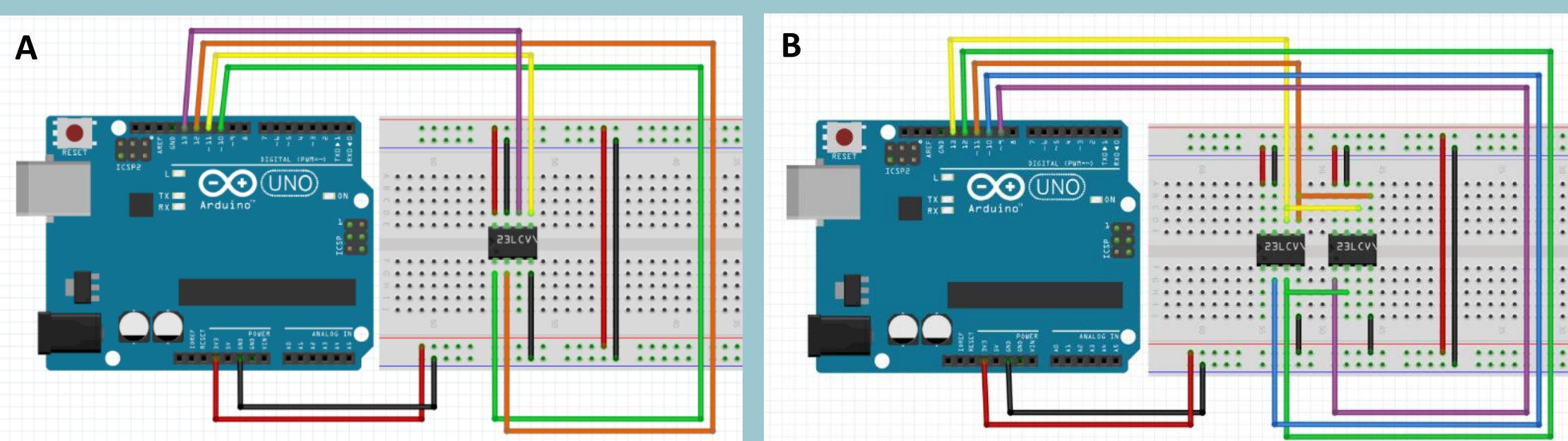- For each additional SRAM connected in parallel an extra CS line is required.

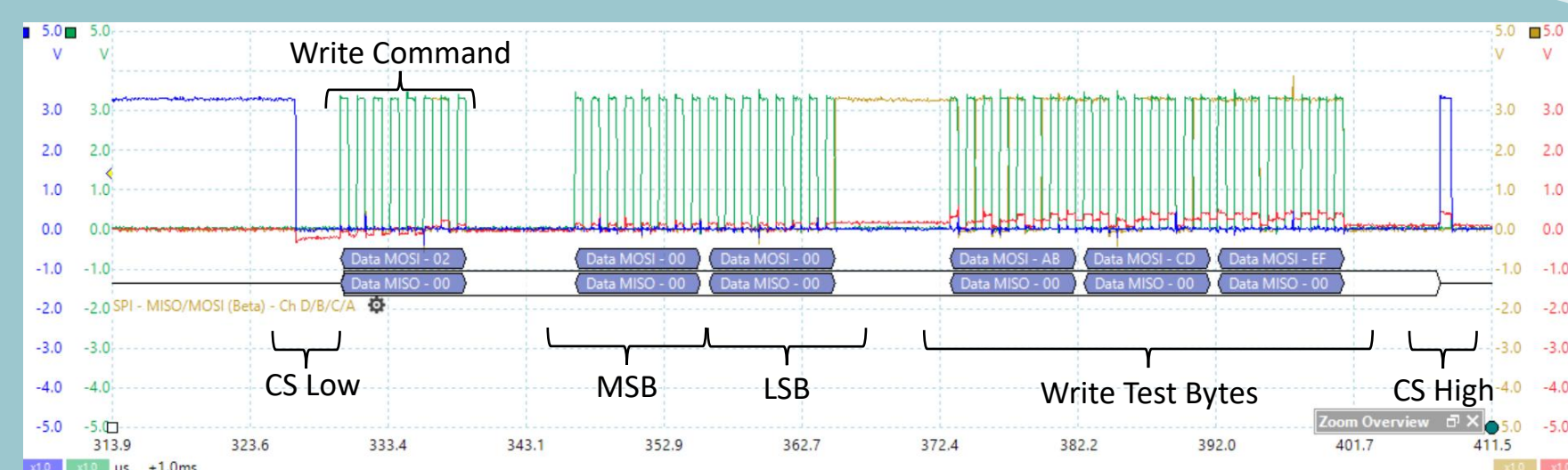*Figure 5: A) Single SRAM circuit, B) Two SRAMs connected in parallel*

Figure 6: Waveforms of a write cycle to the SRAM. ▨: CS line ▨: MISO line ▨: SCK line ▨: MOSI line

Figure 7: Waveform of a read cycle to the SRAM

Nucleo-144 Development Board:

After initial testing, further development was undertaken using the Nucleo-144 development board due to its increased processing power and higher internal memory capacity.
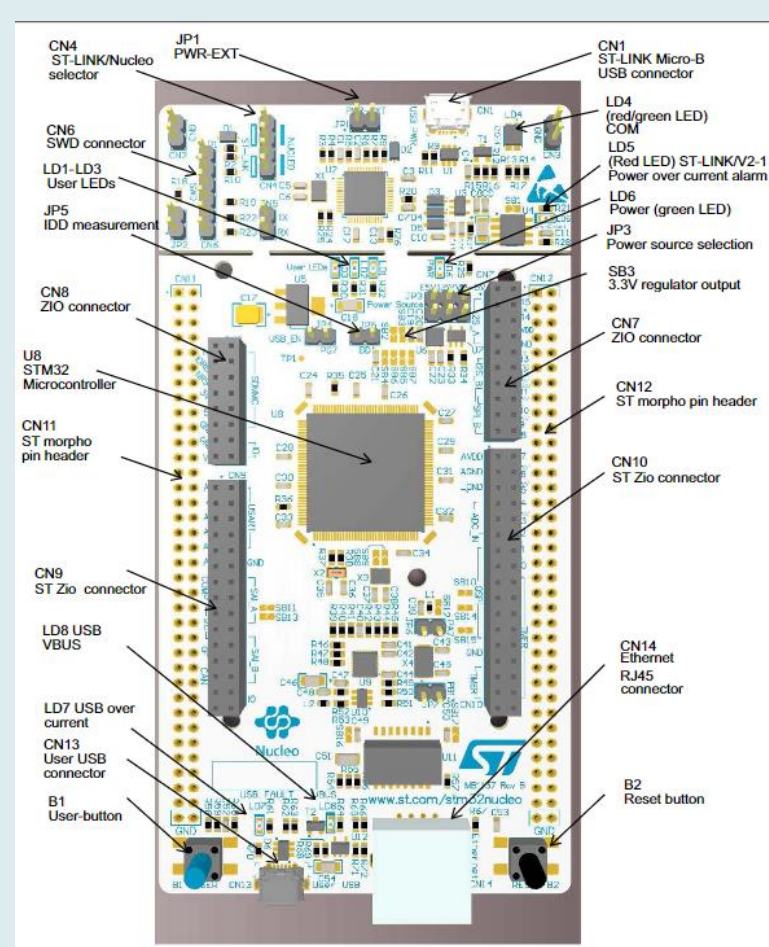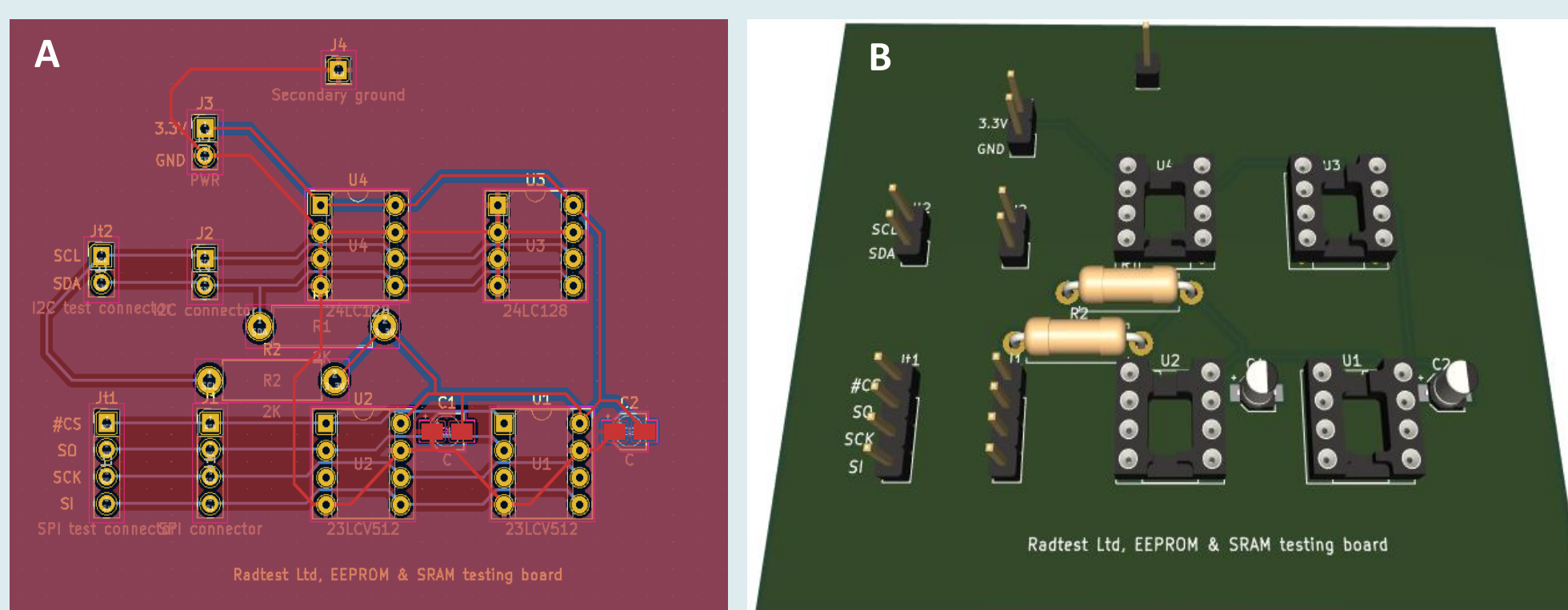
Figure 8: Nucleo-144 Development Board [3]

Figure 8: A) Daughterboard wiring schematic, B) Daughterboard 3D model

DUT Daughterboard Design:

- The daughterboard is designed to allow the simultaneous testing of 4 memories.
- It enables 2 EEPROMs and 2 SRAMs to be tested and is compatible both the heavy ion and laser testing equipment

Follow Link For Digital Access:

References:

[1] Microchip Technology Inc, "128-Kbit I^2C Serial EEPROM", 25LC128 datasheet, Sept 2010.
[2] Microchip Technology Inc, "512-Kbit Serial SRAM with Battery Backup and SDI Interface" 23LCV512 datasheet, Nov 2012.
[3] STMicroelectronics, "UM1974 User Manual", Nucleo-144 datasheet, Aug 2020.

Acknowledgements: